WHAT IS CLAIMED IS

1. A method of making a Wheatstone bridge circuit for a sensor, comprising:

forming first and second sensor elements by forming first and second elongated n type nano width regions on a suitable substrate;

forming third and fourth sensor elements by forming third and fourth elongated p type nano width regions on the substrate; and

interconnecting the first and second sensor elements with the third and fourth sensor elements with conductive connector elements so that the first and second sensor elements are separated from and connected to the third and fourth sensor elements in a manner to form a Wheatstone bridge configuration.

2. A method as set forth in claim 1, wherein the Wheatstone bridge circuit is balanced and wherein the four sensor elements have substantially the same resistance.

3. A method as set forth in claim 1, wherein the sensor elements are substantially equivalent in at least one of length, width, thickness, carrier mobility, carrier concentration, and dielectric thickness.

4. A method as set forth in claim 1, further comprising:

forming the first and second sensor elements so as to have a first predetermined spatial relationship with a centroid; and

forming the third and fourth sensor elements so as to have a second predetermined spatial relationship with the centroid.

5. A method as set forth in claim 4, further comprising forming all the sensor elements to be substantially collinear wherein they are spaced along a line which passes through the centroid.

6. A method as set forth in claim 1, further comprising:

forming a plurality of n type nano width regions in the substrate so that each region is essentially equidistant from and about a centroid and selectively connecting n type nano width regions so as to form the first sensor elements;

forming a second plurality of n type nano width regions in the substrate so that each region is essentially equidistant from and about the centroid and selectively connecting n type nano width regions so as to form the second sensor elements;

forming a plurality of p type nano width regions in the substrate so that each region is essentially equidistant from and about the centroid; and selectively connecting p type nano widt regions so as to form the third sensor elements;

forming a second plurality of p type nano width regions in the substrate so that each regions is essentially equidistant from and about the centroid and selectively connecting selected p type nano width regions so as to form the fourth sensor elements and to cause the third and fourth sensor elements to have essentially the same resistance characteristics as the first and second sensor elements.

7. A method as set forth in claim 1, further comprising:

providing an electrical connection to the substrate, and

providing an appropriate bias such as to substantially negate any average resistance imbalance between the N-type and P-type sensor elements.

8. A method as set forth in claim 1, further comprising:

forming first gate over the first elongated nano width region respectively so as to be separated therefrom by an oxide layer; and

selectively applying a voltage to the gate to negate an imbalance in the bridge circuit.

9. A method as set for in claim 8, further comprising:

forming at least one of second, third, and fourth gates over the second, third and fourth elongated nano width regions respectively so as to be separated therefrom by an oxide layer; and

selectively applying a voltage to at least one of the second, third and fourth gates to negate an imbalance in the bridge circuit.

10. A method as set forth in claim 1, further comprising:

forming a plurality of gates over each of the first and second elongated n type nano width regions so as to be separated therefrom by an oxide layer;

forming a plurality of gates over each of the third and fourth elongated p type nano width regions so as to be separated therefrom by an oxide layer, and

selectively applying a voltage to at least one of the gates to negate an imbalance in the bridge circuit.

11. A method as set forth in claim 1, further comprising: configuring the first sensor element to be responsive to a particular external stimulus of chemical or non-chemical nature.

12. A method as set forth in claim 11, further comprising: configuring the third sensor elements to be responsive in the same way as the first resistor to the external stimulus.

13. A method as set forth in claim 12, further comprising configuring the second and fourth sensor elements to be responsive in a manner which is opposite to the manner in which the first sensor element is responsive to the external stimulus.

14. A Wheatstone bridge circuit for a sensor, comprising:

first and second sensor elements which respond to a stimulus generated when the sensor is exposed to a sample to be measured, the first and second sensor elements comprising first and second elongated n type nano width regions formed in a suitable substrate;

third and fourth sensor elements which respond to the stimulus generated when the sensor is exposed to the sample to be measured, comprising third and fourth elongated p type nano width regions formed in the substrate; and

interconnections which interconnect the first and second sensor elements with the third and fourth sensor elements so that the first and second sensor elements are separated from and connected to the third and fourth sensor elements in a manner to form a Wheatstone bridge configuration.

15. A Wheatstone bridge as set forth in claim 14, wherein the p type and n type nano width regions are formed of a semiconducting material selected from the group consisting of silicon, germanium, diamond, SiC, Si-Ge alloy, GaAs, other III-V compounds, GaN, other II-VI compounds, SnO, other metal oxide semiconducting materials, and wherein the p type and n type sensor elements are chemically doped so as to be p type and n type elements.

16. A Wheatstone bridge as set forth in claim 14, wherein the four sensor elements have substantially equal resistance characteristics and thus substantially balance the Wheatstone bridge.

17. A Wheatstone bridge circuit as set forth in claim 14, further comprising means for balancing the bridge circuit.

18. A Wheatstone bridge as set forth in claim 14, wherein the sensor elements comprise P-type and N-type sensor elements which are formed on a substrate which is configured to be biased to balance the P-type and N-type sensor elements.

19. A Wheatstone bridge as set forth in claim 14, wherein the substrate comprises a semiconducting top layer of submicron thickness that is separated by an insulating layer from an underlying conducting layer that is configured to be electrically biased.

20. A Wheatstone bridge circuit as set forth in claim 14, wherein the first and second sensor elements are essentially equidistant from a centroid, and wherein the third and fourth sensor elements are essentially equidistant from the centroid.

21. A Wheatstone bridge circuit as set forth in claim 14, wherein the sensor elements are arranged collinearly.

22. A Wheatstone bridge circuit as set forth in claim 14, wherein the sensor elements share a common centroid.

23. A Wheatstone bridge circuit for a sensor comprising:

a plurality of n type nano width regions which are arranged in a predetermined spatial relationship and wherein first and second groups of n type nano width regions, which share a common centroid, are respectively connected to form two n type sensor elements which have essentially the same resistance; and

a plurality of p type nano width regions which are arranged in a predetermined spatial relationship and wherein first and second groups of p type nano width regions, which share the same common centroid, are respectively connected to form two p type sensor elements which have essentially the same resistance as the two n type sensor elements.

24. A Wheatstone bridge circuit as set forth in claim 23, comprising: a first gate formed over one of the nano width regions and separated therefrom by an oxide layer, the gate being configured to have a voltage selectively applied thereto to negate an imbalance in the bridge circuit.

25. A Wheatstone bridge circuit as set forth in claim 24, further comprising:

at least one of second, third, and fourth gates formed over portions of other elongated nano width regions respectively so as to be separated therefrom by an insulating dielectric layer;

the first, second, third and fourth gates being respectively configured to have a voltage applied thereto in a manner which negates an imbalance in the bridge circuit.

26. A Wheatstone bridge circuit as set forth in claim 23, further comprising:

a plurality of gates each arranged over an elongated n type nano width regions; and

a plurality of gates each arranged over each of the elongated p type nano width regions, and wherein:

the gates are each being configured to have a voltage applied thereto in a manner which negates an imbalance in the bridge circuit.

27. A half Wheatstone bridge circuit comprising:

a first and second sensor elements that are elongated, balanced, and nanoscale in a direction of their cross-sections, and that respond electrically upon exposure to a stimulus;

a third and forth resistor element that do not respond to the stimulus and have substantially the same resistance as the first and second element; and

interconnections among the elements in a manner to form a half Wheatstone bridge circuit.

28. A half Wheatstone bridge circuit as set forth in claim 27, wherein the third element is configured similarly to the first element, and the fourth element is configured similarly to the second element;

29. A half Wheatstone bridge circuit as set forth in claim 27, wherein the sensor elements are configured to be semiconducting by controlled doping.

30. A half Wheatstone bridge circuit as set forth in claim 27, wherein the sensor elements are nanoscale in two substantially orthogonal cross-sections.

31. A Wheatstone bridge circuit as set forth in claim 29, wherein the first and second sensor elements are similarly doped so as to respond similarly upon exposure to the stimulus.

32. A half Wheatstone bridge circuit as set forth in claim 27, wherein the first and second sensor elements are P and N doped respectively so as to exhibit opposing responses to the stimulus;

33. A half Wheatstone bridge circuit as set forth in claim 27, wherein the first and second sensor elements are doped and fabricated suitably upon a common electrically biasable substrate so the substrate bias acts to balance their resistance.

34. A Wheatstone bridge circuit comprising:

first, second, third and fourth resistors of substantially equal resistance on a substrate; the substrate comprising:

an electrically conducting underlayer and an insulating layer that separates the resistors from the underlayer, the first and second resistors being configured to be semiconducting with P and N type doping respectively; and wherein the substrate is configured to be biased electrically so as to negate any imbalance in the first and second resistances.

35. A Wheatstone bridge circuit as set forth in claim 34, wherein the third and fourth resistors are configured to be semiconducting with P and N type doping respectively; and wherein the substrate is biased electrically so as to negate any imbalance in the third and fourth resistances.

36. A Wheatstone bridge circuit for a sensor, comprising:

first and second resistor elements at least one of which responds to an external stimulus by exhibiting a change in electrical properties, and at least one of which has a nano or micro width;

third and fourth resistor elements; and

interconnections which interconnect the first and second resistor elements with the third and fourth resistor elements so that the first and second resistor elements are separated from and connected to the third and fourth resistor elements in a manner to form a Wheatstone bridge configuration wherein the first and second resistor elements form a first pair of the bridge circuit elements and the third and fourth resistor elements form a second pair of the bridge circuit elements.

37. A Wheatstone bridge circuit as set forth in claim 36, wherein the first and second resistor elements comprise first and second elongated n type regions, and wherein the third and fourth resistor elements comprise elongate p type regions.

38. A Wheatstone bridge circuit as set forth in claim 36, wherein the other of the first and second resistor elements has a nano or micro width.

39. A Wheatstone bridge circuit as set forth in claim 36, wherein at least one of the third and fourth resistor elements has a nano or micro width.

40. A Wheatstone bridge circuit as set forth in claim 36, wherein both of the first and second resistor elements respond to external stimulus by exhibiting a change in electrical properties when exposed to the external stimulus.

41. A Wheatstone bridge circuit as set forth in claim 36, wherein at least one of the third and fourth resistor elements responds to an external stimulus by exhibiting a change in electrical properties.

42. A Wheatstone bridge circuit as set forth in claim 36, wherein both of the third and fourth resistor elements respond to an external stimulus by exhibiting a change in electrical properties.

43. A Wheatstone bridge circuit as set forth in claim 36, wherein at least one of the first, second, third and fourth resistor elements has a micro width and wherein at least one of the first, second, third and fourth resistor elements has a nano width.